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WARNING

Because of possible shock or fire hazards, connection of this instrument should be performed in compliance with the National Electrical Code (ANSI C1) and/or any other requirements which may be applicable to the user.

Installation, operation, and maintenance should be performed only by qualified personnel.

TM-111027

VOLUME 2

SERVICE MANUAL

626-PA-6015

3-CHANNEL TRANSDUCER MONITOR

7 November 1983

(Revised 1 June 1984)

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DESCRIPTION OF REVISIONS*

The following changes have been instituted to reduce the power consumption of this plug-in.
The +16 VDC power supply is now derived from the +12 VDC supply (U17 pin 14). The +12 volt input to U17 is filtered by two 1000uF capacitors, C9 and C22. (See figure 1.) The SYSTEM CHECK reference voltage is derived from the +16 VDC supply. (See figure 2.) The two voltages, VR+ and VR-, used in the ISO AMP offset voltage nulling circuit (R17, R16, R19) are derived from the +12 V and -12 V supplies. (See figure 3.)

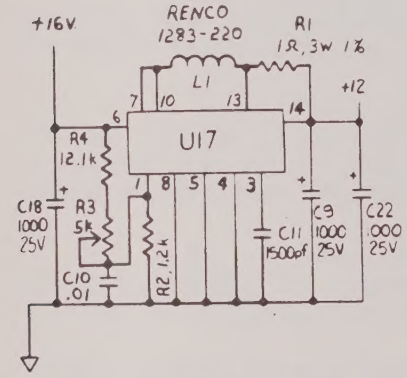


Figure 1.

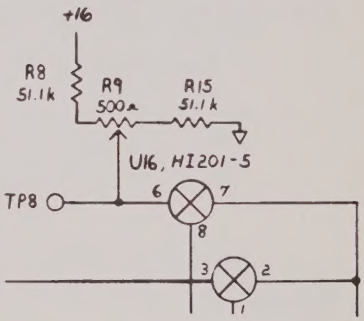
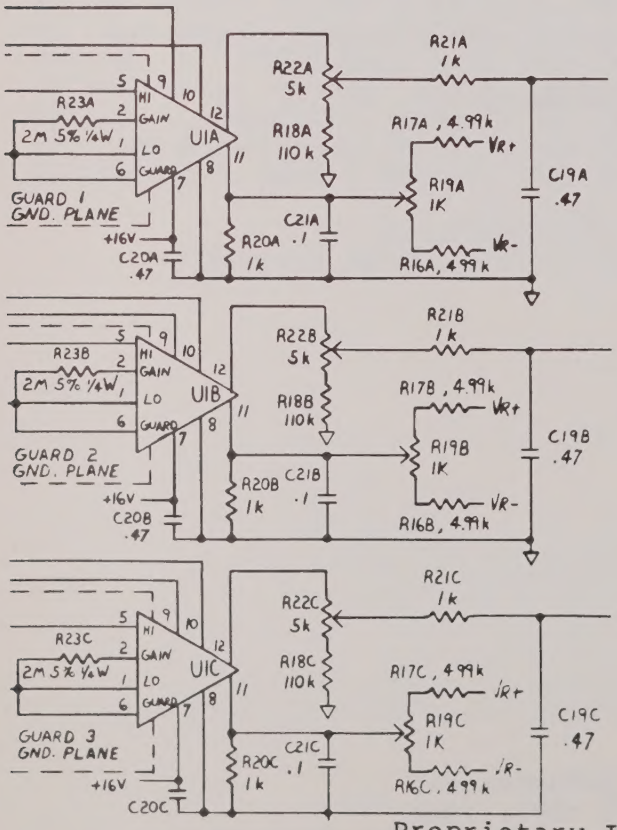


Figure 2.



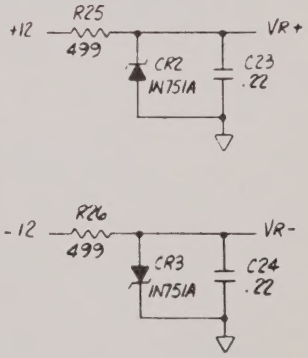


Figure 3.

*Incorporated in pages 4 thru 9

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626-PA-6015 3-CHANNEL TRANSDUCER MONITOR

1 INTRODUCTION

This manual provides maintenance instructions for the 626-PA-6015 3-Channel Transducer Monitor Plug-in which is used in the Model 626 Universal Disturbance Analyzer. Included in this volume are the theory of operation, maintenance, and parts list for the 6015. For operating instructions, refer to Volume 1 of this manual.

2 THEORY OF OPERATION

2.1 Block Diagram Description

The 626-PA-6015 3-Channel Transducer Monitor is designed to monitor three isolated 0 to 10 Vdc inputs. As shown in the block diagram of Figure 1, each of the three inputs is isolated from the others using hybrid isolation amplifiers. The input select circuit feeds the selected signal--Input A, Input B, Input C, or System Check voltage--into the A/D converter circuit. Various decoders, latches, and switches are used to generate the IRQ signal, the A/D converter control signals, and the input select control signals.

2.2 Detailed Circuit Description

The 6015 plug-in, which is built on the transducer input p.c. board (Dranetz 111380), consists of five distinct sections: program storage, control logic, multiplexer circuitry, A/D converter circuitry, and the input circuitry. During normal operation, the three inputs are alternately read, averaged, and compared for threshold and limit crossings. During a system check operation, a known voltage is read and printed out to verify the proper operation of the plug-in board only. The input circuitry calibraton is not checked.

2.2.1 Program Storage Section

The program storage section consists of a 4K x 8 EPROM (U6), a 2K x 8 EPROM (U8) and two 8-bit tristate buffers (U5 and U7). When the software select line MSH(not) goes low, EPROM U6, located at $2XXX, $4XXX, ...etc., depending upon which slot the board is plugged into, is selected and tristate buffer U5 is turned on. EPROM U8, located at $1800-$1FFF, $3800-$3FFF, ...etc., again, depending upon which slot the board is plugged into, is selected and buffer U7 is turned on when MSL(not) goes low and A11 is high.

2.2.2 Control Logic Section

The control logic section breaks the remaining available address space of the plug-in ($1000-$17FF, $3000-$37FF,..) into two blocks: $X00Y and $X08Y. The $X08Y block is not used. The $X00Y block is further broken down into four control words as defined in Table 1. These signals are generated by a 2-4 decoder (U13) using A0, A1, and the proper enabling signal.

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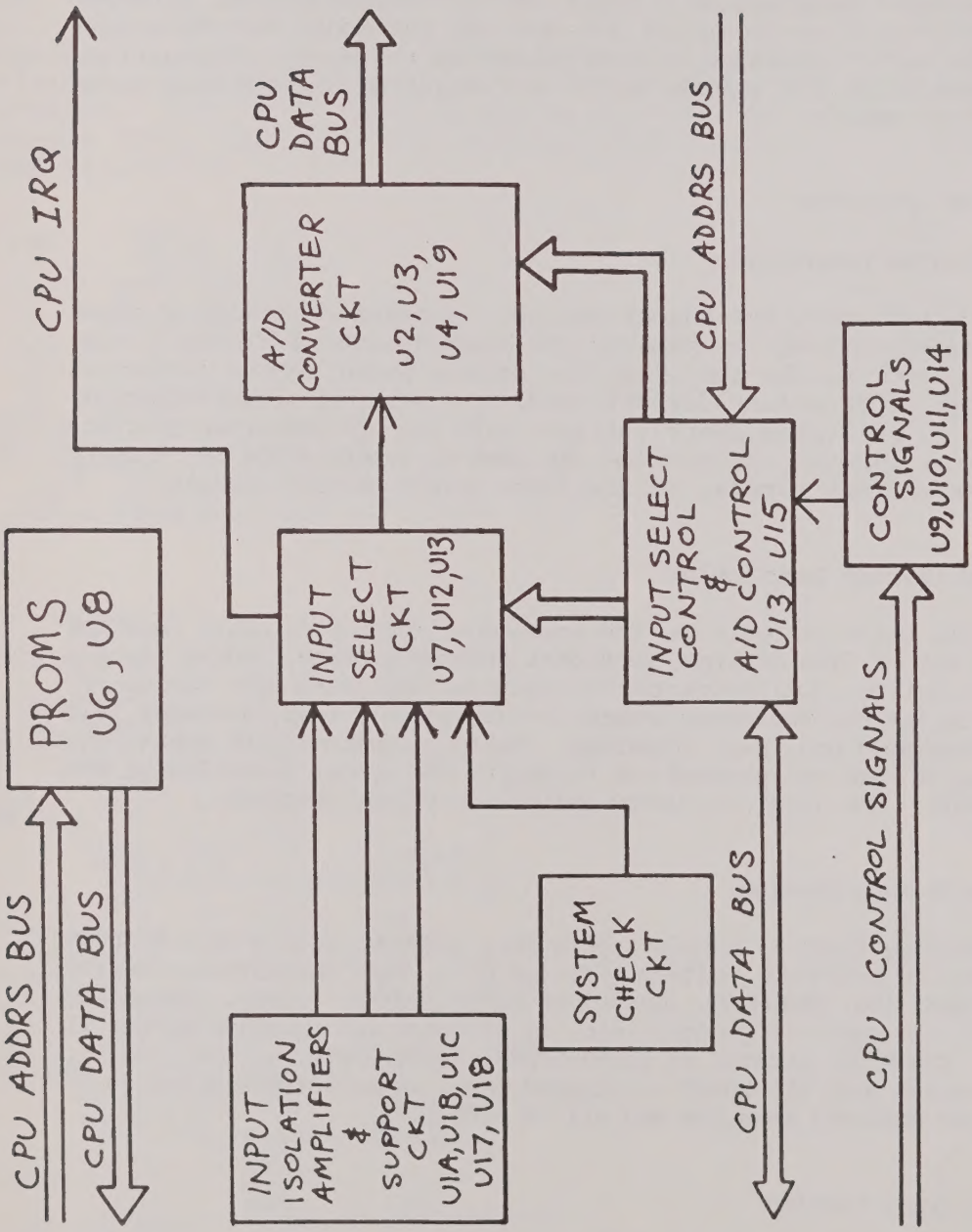
CPU IRQ
CPU DATA BUS
A/D CONVERTER CKT U2, U3, U4, U19
CPU ADDRS BUS
PROMS U6, U8
INPUT SELECT CKT U7, U12, U13
INPUT SELECT CONTROL & A/D CONTROL U13, U15
CONTROL SIGNALS U9, U10, U11, U14
CPU ADDRS BUS
CPU DATA BUS
INPUT ISOLATION AMPLIFIERS & SUPPORT CKT U1A, U1B, U1C U17, U18
SYSTEM CHECK CKT
CPU DATA BUS
CPU CONTROL SIGNALS

Figure 1. 6015, Block Diagram

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Table 1
Address Code

Address	Function
$X000	Mux Latch Clock signal
$X001	Blank & Convert Strobe to ADC
$X002	MSB of ADC data
$X003	LSB of ADC data

The $X000 output of decoder U13 is fed into one-shot U15, and then ORed with the MYW signal, guaranteeing that the latch data is clocked into the 4-bit latch (U12) at the proper time--during write cycles only at approximately 400 nsec from the edge of the Phase 2 clock. The latch contains the encoded multiplexer select values in DB0 and DB1, and the IRQ state in DB7. The IRQ signal is inverted to produce the IRQ(not) signal required by the CPU. The 2 multiplexer data bits are decoded by the remaining half of U13 to produce four switch select lines, defined in Table 2, which are used to enable one switch at a time of U16.

Table 2
Latch Data Code

DB1,0	Function
0 0	Input A
0 1	Input B
1 0	Input C
1 1	System Check

The remaining half of one-shot U15 (address $X001) uses the RC time constant of C14 and R6 to send a Blank and Convert Strobe pulse of approximately 2.5 usec to the A/D.

The system check voltage is derived from the +12 Vdc supply by fixed resistors R8 and R15 and variable resistor R9. This voltage is used during the system check mode to verify that the control circuitry, switch networks and A/D converter section are operational. It does not check the calibration of any input circuit.

2.2.4 A/D Converter and MUX Circuits

During normal operation, the three input signals are alternately selected to pass through the switches of U16, through buffer Op Amp U19 then into the A/D where they are converted to digital form, which can then be read by the CPU. Op Amp U19 is a unity gain buffer with a diode clamp to ground (CR1) on the input. The output of U19 feeds into current setting resistor R10 and variable resistor R12 before entering the A/D. The resistors are used to set the 10 V full scale value to an equivalent ADC output of 1024.

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Upon receiving a convert signal, the A/D converts the selected input signal into 10-bit digital form. The conversion normally takes 25 usec, with a software timer trapping out if it takes too long. The A/D signals completion of the conversion by pulling the Data Ready (not) line low. This status is monitored by the CPU by reading DB7 of the MSB of the data through tristate buffer U3. The lower 2 bits (DB0, DB1) contain the high byte data of the converted data when the Data Ready line is TRUE. The remaining gates of U3 and those of U2 are used to read the lower eight bits of the converted data. These outputs are put on the data bus by selecting the appropriate input to decoder U13.

2.2.5 Input Circuitry

The input section consists of three identical circuits. Identical parts use the same part designations followed by an input identifying suffix--A, B, or C, to indicate the respective input. Each input has its own hybrid isolation amplifier (ISO AMP), U1A, U1B, and U1C, to provide good isolation and high common mode rejection.

The ISO AMPs require a +16 Vdc power supply which is derived from the +12 Vdc supply using the step-up switching regulator circuit of U17. Filtering of the +12 V input is provided by C9 and C22 with filtering of the +16 V output provided by C18. The +16 V level is set by resistor divider network of fixed resistors R2 and R4 and variable resistor R3. Resistor R1 provides input (switching) current limiting, inductor L1 provides switching current (energy) storage, and capacitors C10 and C11 provide additional filtering. The 2-phase clock signal required by the ISO AMPs is provided by the oscillator circuit of U18. Components C16, R13, and variable resistor R11 set the oscillator frequency to approximately 100 KHz +/-5 KHz.

On the input side of the ISO AMPs, U1(A, B, C), the guard and low inputs are connected together, with a separate pin providing connection to frame (chassis) ground. Resistor R24 lowers the input impedance to reduce extraneous noise pick-up when the inputs are open circuited. Resistor R23 provides a small gain increase above 1:1. The resistor divider formed by R22 and R18 is used to compensate for any variations in R23 and bring the gain back down to 1:1. (R22/R18 divider gain : (110K+ .5*5K)/(110K+5K)=.978, typical.) The output from the divider is filtered by R21 and C19 before going into the appropriate analog switch (U16) connection.

The offset voltage of the ISO AMPs is nulled out by fixed resistors R17, R16 and variable resistor R19 and filtered by C21 and R20. Additional power supply filtering is provided by C20.

3 REPLACEABLE PARTS LIST

The replaceable parts list identifies the replaceable parts in the plug-in. The following is presented for each such part: reference designation (if applicable), part number, manufacturer's code number, and a description. Figure 2 identifies the parts on printed circuit board A1.

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REPLACEABLE PARTS LIST

626-PA-6015

PC Board, Transducer Input P/N 111380

REF DESIG	PART NO.	MAN CODE NO.	DESCRIPTION
C1-C8, C12, C15, C17, C23, C24	103209-G2	23207	Cap, .22uF +/-20%, 50V
C9, C22	104075-G3	23207	Cap, 1000uF +/-20%, 10V
C10	104071-G4	23207	Cap, .01uF +/-20%, 400V
C11	104025-G7	23207	Cap, 680pF +/-5%, 100V
C13	104019-G5	23207	Cap, 330pF +/-5%, 500V
C14	104023-G2	23207	Cap, 82pF +/-2%, 500V
C16	104025-G1	23207	Cap, 1000pF +/-5%, 500V
C18	104075-G2	23207	Cap, 470uF +/-20%, 25V
C19A, C19B, C19C	104071-G3	23207	Cap, .47uF +/-20%, 100V
C20A, C20B, C20C	103209-G3	23207	Cap, .47uF +/-20%, 50V
C21A, C21B, C21C	103209-G1	23207	Cap, .1uF +/-20%, 50V
CR1	104412-G2	23207	Diode
CR2, CR3	104403-G6	23207	Diode, Zener, 5.1v
L1	104650-G1	23207	Choke, 220uH
R1	104766-G2	23207	Res, 1 +/-1%, 3W
R2	RN60C1211F		Res, 1.2K +/-1%, 1/8W
R3	104719-G2	23207	Res Var, 5K +/-10%, 1/2W
R4	RN60C1212F		Res, 12.1K +/-1%, 1/8W
R5	RN60C1002F		Res, 10K +/-1%, 1/8W

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REPLACEABLE PARTS LIST (Cont'd)

626-PA-6015

PC Board, Transducer Input P/N 111380

REF DESIG	PART NO.	MAN CODE NO.	DESCRIPTION
R6, R16A, R16B, R16C, R17A, R17B, R17C	RN60C4991F		Res, 4.99K +/-1%, 1/8W
R7, R14	RN60C2001F		Res, 2K +/-1%, 1/8W
R8, R15	RN60C5112F		Res, 5.1K +/-1%, 1/8W
R9, R19A, R19B, R19C	104701-G6	23207	Res Var, 500 +/-10%, 1/2W
R10	RN60C1000F		Res, 100 +/-1%, 1/8W
R11, R22A, R22B, R22C	104701-G7	23207	Res Var, 5K +/-10%, 1/2W
R12	104700-G2	23207	Res Var, 100 +/-10%, 1/2W
R13	RN60C9091F		Res, 9.09K +/-1%, 1/8W
R18A, R18B, R18C	RN60C1103F		Res, 110K +/-1%, 1/8W
R20A, R20B, R20C, R21A, R21B, R21C	RNC60C1001F		Res, 1K +/-1%, 1/8W
R23A, R23B, R23C	RCRO7F205J		Res, 2M +/-5%, 1/4W
R24A, R24B, R24C	RCRO7GF106J		Res, 10M +/-5%, 1/4W
R25, R26	RN60C4990F		Res, 499 +/-1%, 1/8W
U1A, U1B, U1C	104281-G1	23207	IC, Isolation Amplifier
U2,U3	104216-G3	23207	IC, Hex Tri-state Buffer
U4	104365	23207	IC, 10-bit A/D Converter
U5, U7	104225-G5	23207	IC, Octal Buffer
U9,U11	104220-G4	23207	IC, Quad 2-input OR Gate

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REPLACEABLE PARTS LIST (Cont'd)

626-PA-6015

PC Board, Transducer Input P/N 111380

REF DESIG	PART NO.	MAN CODE NO.	DESCRIPTION
U12	104202-G3	23207	IC, Quad D-Latch
U13	104221-G7	23207	IC, Dual 1 of 4 Decoder
U14	104214-G1	23207	IC, Quad 2-input NAND Gate
U15	104216-G6	23207	IC, Dual Multivibrator
U16	104362	23207	IC, Quad Switch
U17	104321	23207	IC, Power Supply Inverter
U18	104206-G3	23207	IC, Hex Schmitt Trigger
U19	104236-G2	23207	IC, Dual Op Amp
XU4	104931	23207	IC Socket, 20 Pin
XU6, XU8	104933	23207	IC Socket, 24 Pin

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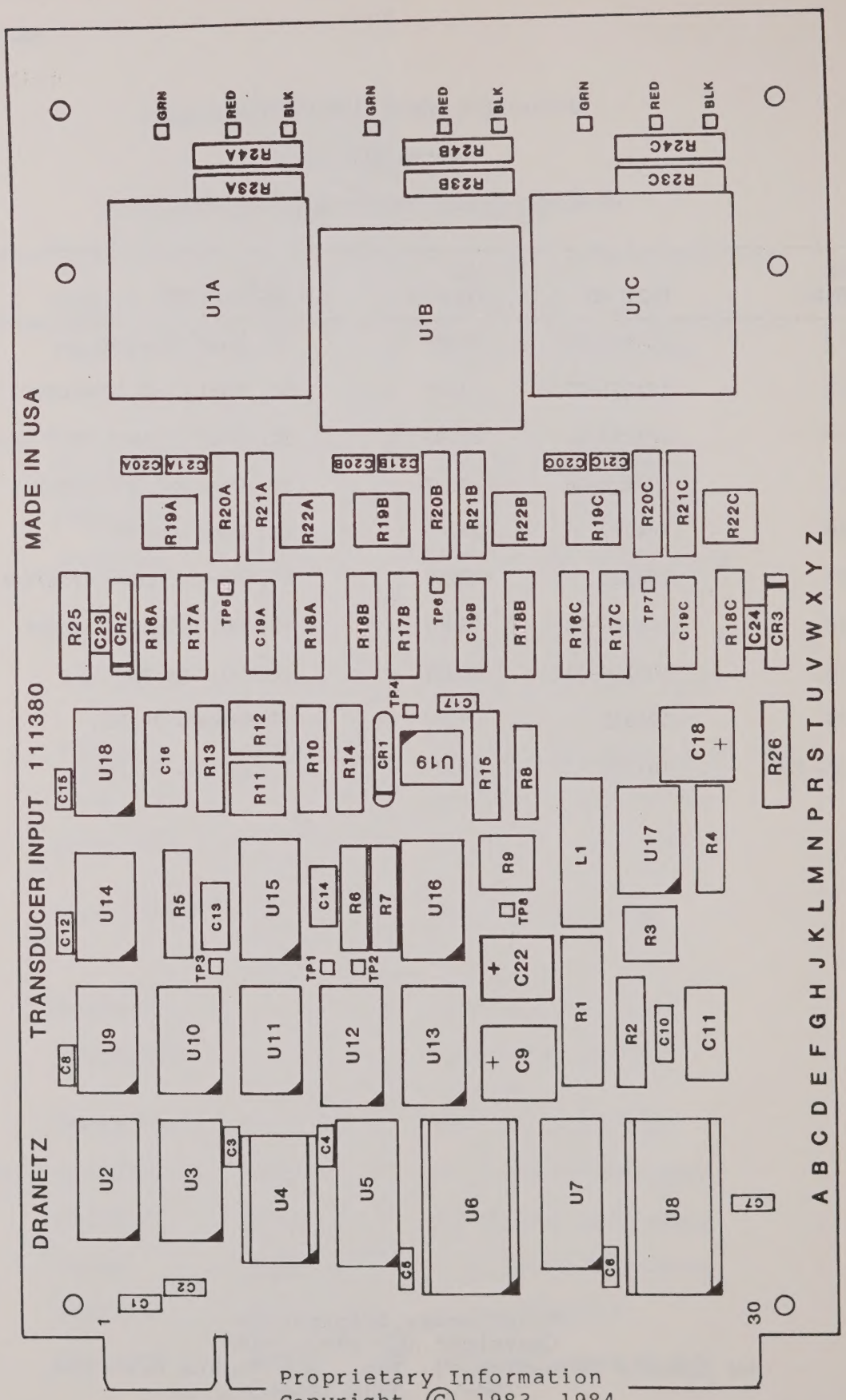

Figure 2. 6015 PC Board, Parts Location

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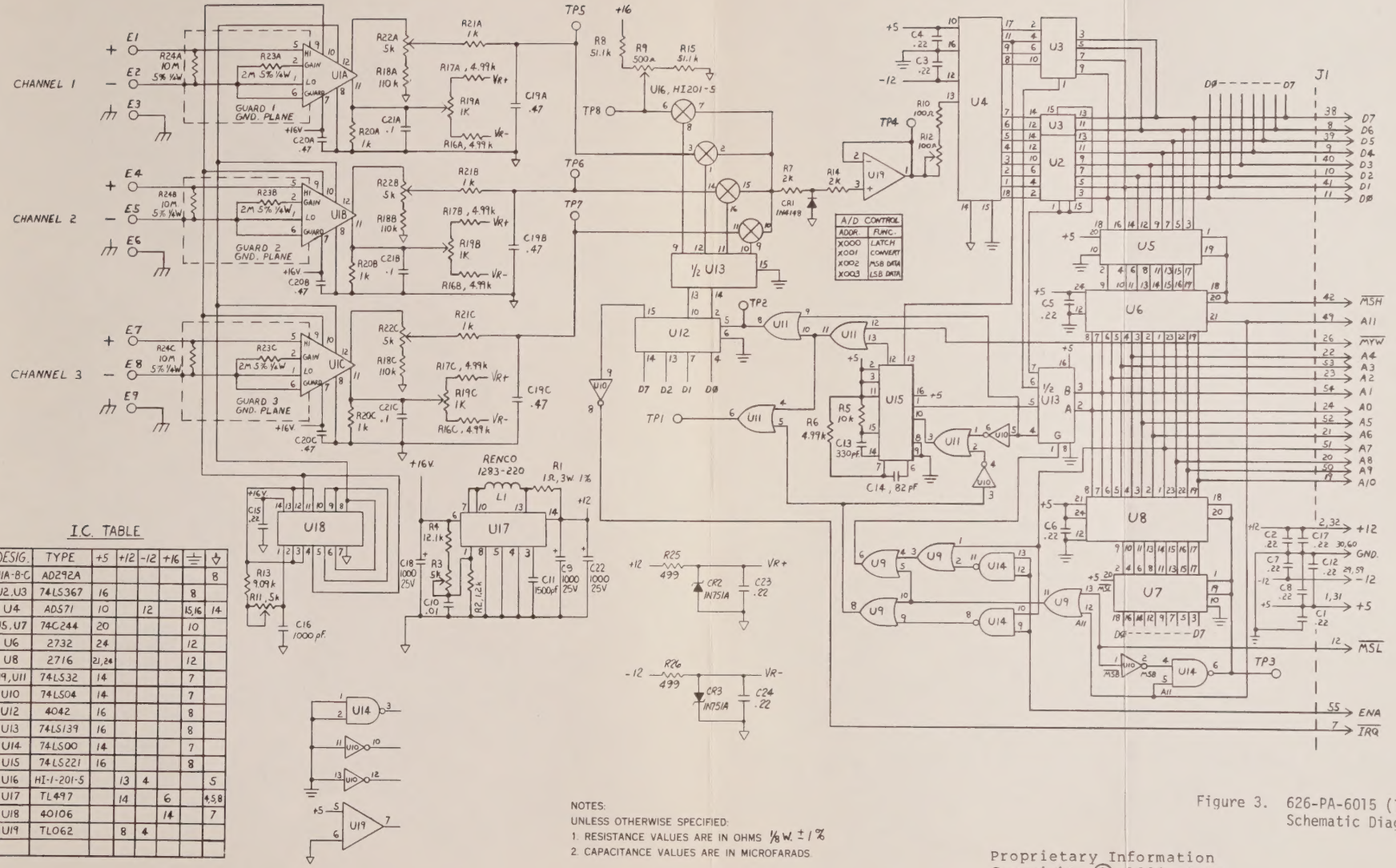

I.C. TABLE

DESIG.	TYPE	+5	+12	-12	+16	⏚	⏚
U1A-B-C	AD292A						8
U2.U3	74LS367	16				8	
U4	AD571	10		12		15,16	14
U5.U7	74C244	20				10	
U6	2732	24				12	
U8	2716	21,24				12	
U9,U11	74LS32	14				7	
U10	74LS04	14				7	
U12	4042	16				8	
U13	74LS139	16				8	
U14	74LS00	14				7	
U15	74LS221	16				8	
U16	HI-1-201-5		13	4			5
U17	TL497		14		6		4,5,8
U18	40106				14		7
U19	TL062		8	4			

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES ARE IN OHMS 1/8 W. ± 1%
2. CAPACITANCE VALUES ARE IN MICROFARADS.

Figure 3. 626-PA-6015 (111380), Schematic Diagram

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